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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,535	02/23/2004	Allen Cheah Chong Leng	ALTRP113/A1350	1525

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EXAMINER	
MATISIAK, JENNIFER E	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,535	LENG ET AL.	
	Examiner	Art Unit	
	Jennifer Matisiak	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-34 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8, 11, 15-24, 31-34 is/are rejected.

7)☒ Claim(s) 9-10,12-14 and 25-30 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 02102006.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 1, 3-6, 15-23, 31-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Smith et al. (US 6538313), hereinafter Smith.

Regarding claim 1, Smith discloses a semiconductor package (Fig. 3A, for example), comprising: a die (120); a wire bonding package substrate (390) positioned under the die, the package substrate having a die attach pad (308) and a plurality of lead fingers (109) surrounding the die attach pad; a plurality of wire bonds (351, 371) electrically connecting the die to the plurality of lead fingers; a bottom plate (107) positioned under the die attach pad; and an insulator (380) set between the die attach pad and the bottom plate such that the die attach pad and the bottom plate are electrically insulated from each other by the insulator.

Regarding claim 3, Smith discloses a semiconductor package further comprising: a molding cap covering at least a portion of the die, package substrate, wire bonds, insulator, and bottom plate (col 1, lines 42-44).

Regarding claim 4, Smith discloses a semiconductor package wherein the die attach pad is larger than the die such that a portion of the die attach pad is exposed around the die (Fig. 3A).

Regarding claim 5, Smith discloses a semiconductor package wherein the bottom plate is larger than the die attach pad such that a portion of the bottom plate is exposed around the die attach pad (Fig. 3A).

Regarding claim 6, Smith discloses a semiconductor package wherein the plurality of wire bonds electrically connects to the exposed portion of the die attach pad (Fig. 3A).

Regarding claims 8 and 11, Smith discloses a device wherein the exposed portion of the bottom plate is capable if being used as an alignment structure. Accordingly, the term "alignment structure" has not been given patentable weight since this is considered to be functional language.

> While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971); *In re Danly,* 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device *is*, not what a device *does*." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909

F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

Regarding claim 15, Smith discloses a semiconductor package wherein the insulator is a non-conductive adhesive tape (col 3, lines 9-10).

Regarding claim 16, Smith discloses a semiconductor package wherein the die is attached to the die attach pad with a die attach epoxy (col 3, lines 10-11).

Regarding claim 17, Smith discloses a semiconductor package wherein the die attach pad is connected to a ground source of the semiconductor package and the bottom plate is connected to a power source of the semiconductor package (col 4, lines 51-54).

Regarding claim 18, Smith discloses a method of assembling a semiconductor package (Fig. 3A), comprising: providing a wire bonding package substrate (390) with a die attach pad (308) and a plurality of lead fingers (109) surrounding the die attach pad, the die attach pad having a top surface and a bottom surface; attaching a die (120) to the top surface of the die attach pad; setting in place an insulator (380) to a bottom plate (107); attaching the bottom plate to the bottom surface of the die attach pad such that the bottom plate and the die attach pad are electrically insulated from each other by the insulator; and electrically connecting a plurality of wire bonds (351, 371) from the die to the plurality of lead fingers.

Regarding claim 19, Smith discloses a method further comprising: forming a molding cap covering at least a portion of the die, package substrate, wire bonds, insulator, and bottom plate (col 1, lines 42-44).

Regarding claim 19, Smith discloses a method further comprising: forming a molding cap covering at least a portion of the die, package substrate, wire bonds, insulator, and bottom plate (col 1, lines 42-44).

Regarding claim 20, Smith discloses a method wherein the die attach pad is larger than the die such that a portion of the die attach pad is exposed around the die (Fig. 3A).

Regarding claim 21, Smith discloses a method wherein the bottom plate is larger than the die attach pad such that a portion of the bottom plate is exposed around the die attach pad (Fig. 3A).

Regarding claim 22, Smith discloses a method further comprising: electrically connecting the plurality of wire bonds to the exposed portion of the die attach pad (Fig. 3A).

Regarding claim 24, Smith discloses the limitations of claim 21. Smith does not explicitly disclose "wherein attaching the bottom plate to the bottom surface of the die attach pad includes aligning the bottom plate with the die attach pad with an alignment structure that is integrated with the exposed portion of the bottom plate." However, it is well known in the art that in order to make a functional semiconductor package, it is required to align a die pad with a bottom plate. Since Smith discloses a method including placing a bottom plate below a die attach pad, the invention of Smith inherently encompasses this limitation of the instant invention.

Regarding claim 31, Smith discloses a method wherein the insulator is a non-conductive adhesive tape (col 3, lines 9-10).

Regarding claim 32, Smith discloses a method wherein the die is attached to the die attach pad with a die attach epoxy (col 3, lines 10-11).

Regarding claim 33, Smith discloses a method wherein the die attach pad is connected to a ground source of the semiconductor package and the bottom plate is connected to a power source of the semiconductor package (col 4, lines 51-54).

Regarding claim 34, Smith discloses a semiconductor package (Fig. 3A) comprising: a die (120); a wire bonding package substrate (390) positioned under the die, the package substrate having a die attach pad (308) and a plurality of lead fingers (109) surrounding the die attach pad; a plurality of wire bonds (351, 371) electrically connecting the die to the plurality of lead fingers; a bottom plate (107) positioned under the die attach pad, wherein the bottom plate and the die attach pad have means for lowering inductance (121); and an insulator (380) set between the die attach pad and the bottom plate such that the die attach pad and the bottom plate are electrically insulated from each other by the insulator.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2, 7, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Lee et al. (US 2004/0159918) hereinafter Lee.

Regarding claim 2, Smith discloses the limitations of claim 1. Smith does not disclose "wherein the package substrate includes a tie bar connected to the die attach pad." Lee discloses a semiconductor package (Figs. 3 and 18, for example), comprising: a die (20); a wire bonding package substrate (101) positioned under the die, the package substrate having a die attach pad (8) and a plurality of lead fingers (10) surrounding the die attach pad; a plurality of wire bonds (24) electrically connecting the die to the plurality of lead fingers; a bottom plate (6) positioned under the die attach pad; and a tie bar (4) connected to the die attach pad. It would have been obvious to one of ordinary in the art at the time the invention was made to include tie bars in the invention of Smith since it is desirable to reduce stress on the die attach pad.

Regarding claim 7, Smith discloses the limitations of claim 6. Smith does not disclose "wherein the plurality of wire bonds electrically connects to the exposed portion of the bottom plate." Lee discloses a semiconductor package (Figs. 3 and 18, for example), comprising: a die (20); a wire bonding package substrate (101) positioned under the die, the package substrate having a die attach pad (8) and a plurality of lead fingers (10) surrounding the die attach pad; a plurality of wire bonds (24) electrically connecting the die to the plurality of lead fingers; a bottom plate (6) positioned under the die attach pad; wherein the plurality of wire bonds electrically connects to the exposed portion of the bottom plate (Fig. 18).

It would have been obvious to one of ordinary in the art at the time the invention was made to electrically connect wire bonds to the expose portions of the bottom plate in the invention of Smith since it is desirable to connect the bottom plate to the power source of the device package.

Regarding claim 23, Smith discloses the limitations of claim 22. Smith does not disclose "further comprising: electrically connecting the plurality of wire bonds to the exposed portion of the bottom plate." Lee discloses a method of assembling a semiconductor package (Figs. 3 and 18, for example) comprising: providing a wire bonding package substrate (101) with a die attach pad (8) and a plurality of lead fingers (10) surrounding the die attach pad, the die attach pad having a top surface and a bottom surface; attaching a die (20) to the top surface of the die attach pad; attaching bottom plate (6) to the bottom surface of the die attach; and electrically connecting a plurality of wire bonds (24) from the die to the plurality of lead fingers.; wherein the plurality of wire bonds electrically connects to the exposed portion of the bottom plate (Fig. 18). It would have been obvious to one of ordinary in the art at the time the invention was made to include tie bars in the invention of Smith since it is desirable to connect the bottom plate to the power source of the device package.

Allowable Subject Matter

3. Claims 9-10, 12-14, 25-28, 29-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer Matisiak whose telephone number is 571-272-2639. The examiner can normally be reached on Business Days 9:30a-6:30p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 517-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEM

DOUGLAS W. OWENS
PRIMARY EXAMINER